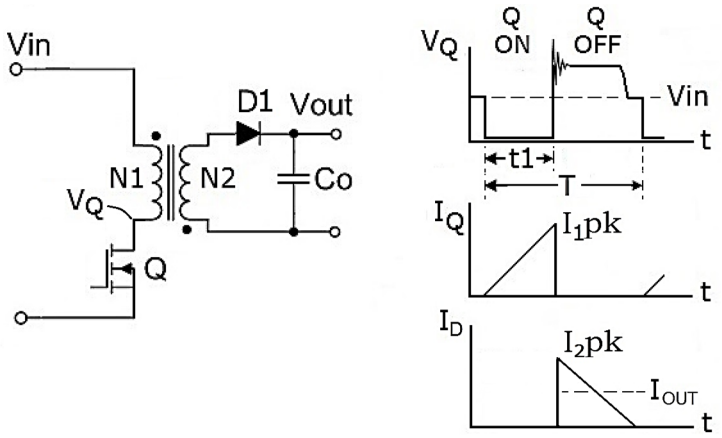
1.9 FLYBACK CONVERTER IN DCM



During ON state of the switch Q, energy is accumulated in the core of the transformer (which acts as an inductor), while output rectifier is reverse biased. During OFF state the transformer releases its entire stored energy. Most of the energy is released via the transformer's secondary into the load and output capacitor Co, the rest is dissipated in snubbers and primary clamp circuit (if any). Switch Q turns ON at zero current but its peak current I_{1PK} is higher than in other topologies.

OUTPUT POWER

In discontinuous conduction mode (DCM) from power balance:

$$Po=\eta\cdot L\mu\cdot I_1pk^2\cdot F/2$$

where $Po=Iout\cdot Vout$ – output power; η - efficiency of the converter; $L\mu$ – transformer's magnetizing (primary) inductance in henry; F- frequency in hertz; I_{1PK}- peak primary current.
Peak primary current is controlled to regulate output voltage.

DUTY CYCLE

In steady-state fixed frequency operation:

$$D=\frac{\sqrt{2P_o\cdot L\mu\cdot F/\eta}}{Vin}$$

where $D=t1/T$ ($D<1$).

OUTPUT VOLTAGE

In steady state: $Vout=\eta Vin^2 \cdot D^2/(2L\mu \cdot F \cdot Iout)$.

TRANSFORMER

Peak primary current: $I_{1PK}=\sqrt{(2Po/\eta \cdot L\mu \cdot F)}$.
Peak secondary current: $I_{2PK}=I_1pk \cdot N1/N2$,
where $N1/N2$ - primary to secondary turns ratio.

If DCM is desired over entire input voltage range:

$$L\mu < \frac{\eta \cdot V_{IN\_MIN}{}^2 \cdot D_{LL}{}^2}{2Po \cdot F}$$

where D_{LL} – desired maximum duty cycle at low line ($D_{LL} < Dmax$, where $Dmax$ – maximum duty cycle of PWM controller).
In most controllers $Dmax$ is 0.45 to 0.99. If $Dmax$ is close to 1.0, it is common to set D_{LL} around 0.7 to limit maximum FET voltage.
For selected $L\mu$, duty cycle at low line:

$$D_{LL} = \frac{\sqrt{2P_o \cdot L\mu \cdot F/\eta}}{V_{IN\_MIN}}$$

Turns ratio is usually selected such that at low line and full load the transformer will be near the boundary of DCM and CCM:

$$\frac{N1}{N2} \approx \frac{D_{LL} \cdot V_{IN\_MIN}}{Vout \cdot (1 - D_{LL})}$$

The core's reset time (the time it takes the transformer to completely demagnetize) is given by:

$$t_{RESET} = \frac{L\mu \cdot I_1pk}{(N1/N2) \cdot Vout}$$

RMS value of primary current: $I_{1\_RMS}=I_{1PK} \cdot \sqrt{(D/3)}$.

It reaches maximum at low line:

$$I_{1\_RMS\_MAX} = \sqrt[4]{\frac{8 \cdot Po^3}{9 \cdot L\mu \cdot F \cdot \eta^3 \cdot {V_{IN\_MIN}}^2}}$$

DC component of primary current: $I_{1\_DC}=Vout \cdot Iout/(\eta \cdot V_{IN})$

RMS value of AC component of primary current:

$$I_{1\_AC\_RMS} = \sqrt{{I_{1\_RMS}}^2 - {I_{1\_DC}}^2}$$

RMS value of secondary current:

$$I_{2\_RMS} = I_2 pk \cdot \sqrt{\frac{t_{reset} \cdot F}{3}} = \sqrt[4]{\frac{8 \cdot Po^3 \cdot T^2}{9 \cdot L\mu \cdot F \cdot \eta^3 \cdot {V_{OUT}}^2}}$$

DC component of secondary current: $I_{2\_DC}=Iout$.
RMS value of AC component of secondary current:

$$I_{2\_AC\_RMS} = \sqrt{{I_{2\_RMS}}^2 - Iout^2}$$

The required core and turns are determined by the $N1 \cdot Ac$ product:

$$N1 \cdot Ac = \frac{L\mu \cdot I_1 pk \cdot 10^8}{B_{PK}}$$

where Ac - core's equivalent cross-sectional area in sq.cm, Bpk – desired peak magnetic flux (Gauss).
See POWER INDUCTOR DESIGN (chapter 4.4) for selecting core size.
Since in flyback the magnetizing current is primary current, an air gap must be introduced in ferrite cores to prevent the magnetic material saturation:

$$lg = \frac{0.4 \cdot \pi \cdot N1 \cdot I_1 pk}{B_{PK}} - \frac{lm}{\mu_r}$$

where lg – net length of air gap (cm), lm – effective magnetic core path length (cm), μ_r – relative permeability of ungapped core.

SWITCH Q

Peak current: $I_{Q\_PK}=I_{1PK}$;

Conduction losses: $P_{Q\_COND} = I_1rms^2 \cdot R_{dson}$, where R_{dson} - drain to source resistance of Q in on-state.
Peak plateau voltage: $V_{Q\_pk} = V_{IN\_MAX} + Vout \cdot N1/N2$.

Note. Instantaneous peak voltage can exceed the plateau by severalfold due to spikes caused by leakage inductance. Its actual value depends on the leakage inductance, primary snubber and clamp circuit (if any). As a rule of thumb, we select the MOSFET with rated voltage 2-3 greater than V_{Q_PK}. Otherwise we can use flyback either with two switches or with active clamp reset (see 1.11) that limits V_{Q_PK} .
If PWM controller limits switch peak current to I_{PK_LIM}, maximum achievable load current for given $Vout$:

$$I_{OUT\_MAX} = \frac{\eta \cdot L\mu \cdot F \cdot I_{PK\_LIM}{}^2}{2 \cdot Vout}$$

RECTIFIER D1

Peak current: $I_{D\_PK} = I_{2PK}$;
Average current: $I_{D}\_av = Iout$;
Reverse voltage plateau: $V_{D\_PK} = Vout + V_{IN\_MAX} \cdot N2/N1$.

Note. Instantaneous peak voltage can exceed the plateau by severalfold due to spikes caused by leakage inductance. As a rule of thumb, we select the diode with rated voltage 2-3 times greater than voltage plateau V_{D_PK}.

OUTPUT CAPACITOR Co

RMS current:

$$Ic\_rms = \sqrt{I_2rms^2 - Iout^2}$$

Net output capacitance is selected to satisfy ripple requirements (see Chapter 5.2) and transient response (see Chapter 5.3).

INPUT CURRENT

Average input current: $I_{IN\_AV} = Vout \cdot Iout/(\eta \cdot Vin)$;
AC component of input current, which is current through input capacitor (not shown on the diagram): $I_{IN\_AC\_RMS} = I_{1\_AC\_RMS}$.